What is claimed is:

1. A gate process for an embedded memory device, comprising the steps of:

providing a semiconductor silicon substrate having a memory cell area and a logic circuit area;

forming a first dielectric layer overlying the semiconductor silicon substrate;

forming a gate structure overlying the first dielectric layer of the memory cell area;

forming a protective layer overlying the first dielectric layer and the top and sidewall of the gate structure;

forming an insulating spacer overlying the protective layer disposed overlying the sidewall of the gate structure;

performing a pre-cleaning process to remove the protective layer and the first dielectric layer overlying the logic circuit area;

forming a second dielectric layer overlying the logic circuit area; and

forming a gate layer overlying the second dielectric layer of the logic circuit area.

2. The gate process for an embedded memory device as claimed in claim 1, wherein the memory cell area comprises a flash memory cell or a DRAM cell.

3. The gate process for an embedded memory device as claimed in claim 1, wherein the first dielectric layer is a silicon oxide layer.

4. The gate process for an embedded memory device as claimed in claim 1, wherein the gate structure overlying the memory cell area comprises:

a floating gate layer formed overlying the first dielectric layer of the memory cell area;

a dielectric structure formed overlying the floating gate layer; and

a control gate layer formed overlying the dielectric structure.

5. The gate process for an embedded memory device as claimed in claim 1, wherein the protective layer is a silicon oxide layer or a silicon nitride layer.

6. The gate process for an embedded memory device as claimed in claim 1, wherein the protective layer has a thickness of 50~500Å.

7. The gate process for an embedded memory device as claimed in claim 1, wherein the pre-cleaning process removes the protective layer and the first dielectric layer disposed outside the insulating spacer overlying the memory cell area.

8. The gate process for an embedded memory device as claimed in claim 1, wherein the second dielectric layer is a silicon oxide layer.

9. The gate process for an embedded memory device as claimed in claim 1, wherein the second dielectric layer is formed overlying the memory cell area.

10. The gate process for an embedded memory device as claimed in claim 1, wherein the formation of the gate layer overlying the logic circuit area comprising the steps of:

depositing a conductive layer overlying the second dielectric layer;

forming a first photoresist layer overlying the conductive layer to cover the logic circuit area;

etching the conductive layer overlying the memory cell area;

removing the first photoresist layer;

forming a second photoresist layer to cover the memory cell area and has a pattern corresponding to the gate layer overlying the logic circuit area;

removing the exposed conductive layer, in which the conductive layer remaining overlying the logic circuit area serves as the gate layer; and

removing the second photoresist layer.

11. A gate structure for an embedded memory device, comprising:

a semiconductor silicon substrate having a memory cell area and a logic circuit area;

a tunnel dielectric layer formed overlying the memory cell area of the semiconductor silicon substrate;

a gate structure formed overlying the tunnel dielectric layer of the memory cell area;

a protective layer formed overlying the tunnel dielectric layer and the sidewall of the gate structure;

an insulating spacer formed overlying the protective layer disposed overlying the sidewall of the gate structure;

a gate dielectric layer overlying the logic circuit area of the semiconductor silicon substrate; and

a gate layer formed overlying the gate dielectric layer of the logic circuit area.

12. The gate structure for an embedded memory device as claimed in claim 11, wherein the memory cell area comprises a flash memory cell or a DRAM cell.

13. The gate structure for an embedded memory device as claimed in claim 11, wherein the tunnel dielectric layer is a silicon oxide layer.

14. The gate structure for an embedded memory device as claimed in claim 11, wherein the gate structure overlying the memory cell area comprises:

a floating gate layer formed overlying the first dielectric layer of the memory cell area;

a dielectric structure formed overlying the floating gate layer; and

a control gate layer formed overlying the dielectric structure.

15. The gate structure for an embedded memory device as claimed in claim 11, wherein the protective layer is a silicon oxide layer or a silicon nitride layer.

16. The gate structure for an embedded memory device as claimed in claim 11, wherein the protective layer has a thickness of 50~500Å.

17. The gate structure for an embedded memory device as claimed in claim 11, wherein the gate dielectric layer is a silicon oxide layer.

18. The gate structure for an embedded memory device as claimed in claim 11, wherein the gate layer is a polysilicon layer.